Course Number and Name

BEC001 - ADVANCED COMPUTER ARCHITECTURE

Credits and Contact Hours

3 and 45

Course Coordinator's Name

Ms C.Geetha

Text Books and References

TEXT BOOKS:

1. Kai Hwang, Advanced Computer architecture Parallelism ,scalablity ,Programmablity , Mc Graw Hill,N.Y, 2003
2. Kai Hwang and F.A.Briggs, Computer architecture and parallel processor ' Mc Graw Hill, N.Y, 1999

REFERENCES:

1. David A. Patterson and John L. Hennessey, —Computer organization and design Elsevier, Fifth edition, 2014.
2. www.sci.tamucc.edu/~sking/Courses/COSC5351/syllabus.php

Course Description

- To make students know about the Parallelism concepts in Programming
- To give the students an elaborate idea about the different memory systems and buses.
- To introduce the advanced processor architectures to the students.
- To make the students know about the importance of multiprocessor and multi-computers.
- To study about data flow computer architectures

Prerequisites	Co-requisites
Principles of digital electronics	Microprocessor & Microcontroller

required, elective, or selected elective (as per Table 5-1)

Selected Elective

Course Outcomes (COs)

CO1: Demonstrate concepts of parallelism in hardware/software.
CO2 : Discuss memory organization and mapping techniques.
CO3 : Describe architectural features of advanced processors.
CO4 : Interpret performance of different pipelined processors.
CO5: Explain data flow in arithmetic algorithms
CO6 : Development of software to solve computationally intensive problems.

Student Outcomes (SOs) from Criterion 3 covered by this Course

COs/SOs	a	b	c	d	e	f	g	h	i	j	k
CO1	H					M				M	
CO2	M	M	H					L			
CO3	M		H	H					H		
CO4	M				H		M				M
CO5		M			M				M		
CO6						H					

List of Topics Covered
UNIT- I **9** **PARALLEL COMPUTER MODELS** Evolution of Computer architecture, system attributes to performance, Multi processors and multi computers, Multi-vector and SIMD computers, PRAM and VLSI models-Parallelism in Programming, conditions for Parallelism-Program Partitioning and Scheduling-program flow Mechanisms-Speed up performance laws-Amdahl's law, Gustafson's law-Memory bounded speedup Model. **UNIT- II** **9** **MEMORY SYSTEMS AND BUSES** Memory hierarchy-cache and shared memory concepts-Cache memory organization-cache addressing models, Aliasing problem in cache, cache memory mapping techniques-Shared memory organization-Interleaved memory organization, Lower order interleaving, Higher order interleaving. Back plane bus systems-Bus addressing, arbitration and transaction. **UNIT -III** **9** **ADVANCED PROCESSORS** Instruction set architectures-CISC and RISC scalar processors-Super scalar processors-VLIW architecture- Multivector and SIMD computers-Vector processing principles-Cray Y-MP 816 system-Inter processor communication **UNIT- IV** **9** **MULTI PROCESSOR AND MULTI COMPUTERS** Multiprocessor system interconnects- Cross bar switch, Multiport memory-Hot spot problem, Message passing mechanisms-Pipelined processors-Linear pipeline, on linear pipeline-Instruction pipeline design-Arithmetic pipeline design. **UNIT- V** **9** **DATA FLOW COMPUTERS AND VLSI COMPUTATIONS** Data flow computer architectures-Static, Dynamic-VLSI Computing Structures-Systolic array architecture, mapping algorithms into systolic arrays, Reconfigurable processor array-VLSI matrix arithmetic processors-VLSI arithmetic models, partitioned matrix algorithms, matrix arithmetic pipelines.